CLAIMS:
What is claimed is:

1. A method for manufacturing and distributing programmable integrated circuits (ICs), comprising the steps of:

placing plural programmable ICs into inventory such that the inventory is re-accessible in an automated manner;

unpacking a subset of the inventoried ICs in order to process an order;

programming the unpacked ICs; and

re-packing the programmed ICs for shipment.

2. The method according to claim 1, further comprising dry packing plural programmable ICs prior to placing the plural programmable ICs into inventory.

3. The method according to claim 1, wherein the ICs comprise field programmable gate arrays (FPGAs) and the step of programming comprises the steps of:

attaching a memory device to the FPGAs; and

programming the FPGAs using a configuration program stored in the memory device.

4. The method according to claim 1, wherein the ICs each comprise a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident in one package and the step of programming comprises the step of:

programming the memory device while it is connected to the FPGA; and

powering up the FPGA and the memory device in order that the memory device configures the FPGA.

5. The method according to claim 1, wherein the ICs each comprise a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident on a common die and the step of programming comprises the step of:

programming the memory device while it is connected to the FPGA; and

powering up the FPGA and the memory device in order that the memory device configures the FPGA.

6. The method according to claim 3, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

7. The method according to claim 4, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

8. The method according to claim 5, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

9. The method according to claim 5, wherein the memory device is an anti-fuse.

10. The method according to claim 1, wherein the step of programming comprises programming the ICs with a pre-verified working configuration.

11. A computer controlled method for processing an order for programmable integrated circuits (ICs), comprising the steps of:

storing a plurality of configurations;

pulling specified volumes of un-programmed ICs from inventory in response to an order from a customer;

programming the specified volumes of ICs with a configuration selected by the customer; and

packing the programmed ICs for shipment.

12. The method according to claim 11, wherein the ICs comprise field programmable gate arrays (FPGAs) and the step of programming comprises the steps of:

attaching a memory device to the FPGAs; and

programming the FPGAs using the selected configuration stored in the memory device.

13. The method according to claim 11, wherein the ICs each comprise a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident in one package and the step of programming comprises the step of:

programming the memory device while it is connected to the FPGA; and

powering up the FPGA and the memory device in order that the memory device configures the FPGA.

14. The method according to claim 11, wherein the ICs each comprise a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident on a common die and the step of programming comprises the step of:

programming the memory device while it is connected to the FPGA; and

powering up the FPGA and the memory device in order that the memory device configures the FPGA.

15. The method according to claim 12, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

16. The method according to claim 13, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

17. The method according to claim 14, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

18. The method according to claim 14, wherein the memory device is an anti-fuse.

19. The method according to claim 11, further comprising the step of testing the programmed ICs.

20. The method according to claim 11, further comprising the step of labeling the programmed ICs to reflect the selected configuration.

21. The method according to claim 11, further comprising tracking sales of the volumes of ICs programmed using the specific configuration.

22. The method according to claim 11, wherein the selected configuration is developed by the customer.

23. The method according to claim 20, wherein the step of labeling comprises marking the programmed ICs with at least one of a customer name and a customer logo.

24. A method for programming an integrated circuit (IC) including an on-chip decryptor, comprising the steps of:

encrypting a configuration program;

loading the encrypted configuration program onto the IC as a bitstream;

loading a decryption key co-resident into the IC in an externally write only, battery backed, memory location;

decrypting the incoming bitstream using the on-chip decryptor with the decryption key in order to recreate the chip configuration program; and

initializing the IC for operation using the decrypted configuration program.

25. A method for programming an integrated circuit (IC) including an on-chip decryptor, comprising the steps of:

encrypting a configuration program;

loading the encrypted configuration program onto the IC as a bitstream;

loading a decryption key co-resident onto the IC in an externally write only memory location;

decrypting the incoming bitstream using the on-chip

decryptor with the decryption key in order to recreate the chip configuration program; and

initializing the IC for operation using the decrypted configuration program.

26. A method for programming an integrated circuit (IC), comprising the steps of:

encrypting a configuration program using an algorithm;

loading the encrypted configuration program onto the IC as a bitstream;

loading a decryption program for said algorithm co-resident into the IC;

loading a decryption key co-resident into the IC in an externally write only, battery backed, memory location;

initializing the IC using the decryption program for said algorithm;

decrypting the incoming bitstream using the decryption program for said algorithm with the decryption key in order to recreate the chip configuration program; and

initializing the IC for operation using the decrypted configuration program.

27. A method for programming an integrated circuit (IC), comprising the steps of:

encrypting a configuration program using an algorithm;

loading the encrypted configuration program onto the IC as a bitstream;

loading a decryption program for said algorithm co-resident into the IC;

loading a decryption key co-resident into the IC in an external write only memory location;

initializing the IC using the decryption program for said algorithm;

decrypting the incoming bitstream using the decryption program for said algorithm with the decryption key in order to recreate the chip configuration program; and

initializing the IC for operation using the decrypted configuration program.

28. The method according to claim 15, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, electrically erasable PROM, and an anti-fuse.

29. A system for processing an order for programmable integrated circuits (ICs), comprising:

means for storing a plurality of configurations;

means for pulling specified volumes of un-programmed ICs from inventory in response to an order from a customer;

means for programming the specified volumes of ICs with a configuration selected by the customer;

means for packing the programmed ICs for shipment; and

computerized means for controlling the means for pulling, programming, and packing.

30. The system according to claim 29, wherein the ICs include field programmable gate arrays (FPGA) and the means for programming comprises:

means for attaching a memory device to the FPGA and programming the FPGA using the selected configuration stored in the memory device.

31. The system according to claim 29, wherein the ICs each include a field programmable gate array (FPGA) and a memory device connected to the FPGA, the means for programming programs the memory device while it is connected to the FPGA, and the system further comprises:

means for powering up the FPGA and the memory device in order that the memory device configures the FPGA.

32. The system according to claim 29, wherein the ICs each include a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident on a common die, the means for programming programs the memory device while it is connected to the FPGA, and the system further comprises:

means for powering up the FPGA and the memory device in order that the memory device configures the FPGA.

33. The system according to claim 31, wherein the FPGA and the memory device are co-resident on a common die.

34. The system according to claim 30, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

35. The system according to claim 31, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

36. The system according to claim 32, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

37. The system according to claim 32, wherein the memory device is an anti-fuse.

38. The system according to claim 29, further comprising means for testing the programmed ICs.

39. The system according to claim 29, further comprising means for labeling the programmed ICs to reflect the selected configuration.

40. The system according to claim 29, further comprising means for tracking sales of the volumes of ICs programmed using the specific configuration.

41. The system according to claim 29, wherein the selected configuration is developed by the customer.

42. The system according to claim 39, wherein the means for labeling comprises means for marking the programmed ICs with at least one of a customer name and a customer logo.